IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Jerome M. Eldridge et al.	Examiner:	Tu-Tu Ho
Serial No.:	10/081,818	Group Art Unit:	2818
Filed:	February 20, 2002	Docket:	1303.045US1
Title:	ATOMIC LAYER DEPOSITION OF METAL OXIDE AND/OR LOW ASYMMETRICAL TUNNEL BARRIER INTERPLOY INSULATORS		

INFORMATION DISCLOSURE STATEMENT

Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

In compliance with the duty imposed by 37 C.F.R. § 1.56, and in accordance with 37 C.F.R. §§ 1.97 *et. seq.*, the enclosed materials are brought to the attention of the Examiner for consideration in connection with the above-identified patent application. Applicants respectfully request that this Information Disclosure Statement be entered and the documents listed on the attached Form 1449 be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicants request that a copy of the 1449 form, initialed as being considered by the Examiner, be returned to the Applicants with the next official communication.

Pursuant to 37 C.F.R. §1.97(b), it is believed that no fee or statement is required with the Information Disclosure Statement.

The Examiner is invited to contact the Applicants' Representative at the below-listed telephone number if there are any questions regarding this communication.

Respectfully submitted,

JEROME M. ELDRIDGE ET AL.

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 349-9587

Date 5 Dec '03 By _____

Timothy B. Clise
Reg. No. 40,957

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop RCE, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 5th day of December, 2003.

Amy Moriarty
Name

_____
Signature

PTO/SB/08A(10-01)
Approved for use through 10/31/2002. OMB 651-0031
US Patent & Trademark Office: U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 1

Complete if Known

Application Number	10/081,818
Filing Date	February 20, 2002
First Named Inventor	Eldridge, Jerome
Group Art Unit	2818
Examiner Name	Ho, Tu-Tu

Attorney Docket No: 1303.045US1

US PATENT DOCUMENTS

Examiner Initial *	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	Filing Date If Appropriate
	US-2001/0013621	08/16/2001	Nakazato, K	257	314	12/08/2000
	US-2001/0055838	12/27/2001	Walker, A J., et al.	438	129	08/13/2001
	US-2002/0028541	03/07/2002	Lee, T H., et al.	438	149	08/13/2001
	US-5,691,209	11/25/1997	Liberkowski, J B.	437	7	10/15/1996
	US-5,739,544	04/14/1998	Yuki, K , et al.	257	25	12/12/1995
	US-5,952,692	09/14/1999	Nakazato, K. , et al.	257	321	10/28/1997
	US-6,077,745	06/20/2000	Burns, M S., et al.	438	270	10/29/1997
	US-6,210,999	04/03/2001	Gardner, , et al.	438	183	12/04/1998
	US-6,306,708	10/23/2001	Peng, N	438	266	02/02/2000
	US-6,433,382	08/13/2002	Orlowski, M , et al.	257	315	04/06/1995
	US-6,461,931	10/08/2002	Eldridge, Jerome M.	438	398	08/29/2000
	US-6,475,857	11/05/2002	Kim, W. , et al.	438	240	06/21/2001
	US-6,541,280	04/01/2003	Kaushik, , et al.			03/20/2001
	US-6,586,797	07/01/2003	Forbes, Leonard , et al.	257	325	08/30/2001

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Foreign Document No	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	T[2]

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No [1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
		SHI, Y. , "Tunneling Leakage Current in Ultrathin (<4 nm) Nitride/Oxide Stack Dielectrics", IEEE Electron Device Letters, 19(10), (1998),pp. 388-390	
		ZHANG, "Atomic Layer Deposition of High Dielectric Constant Nanolaminates", Journal of The Electrochemical Society, 148(4),(2001),F63-F66	

EXAMINER **DATE CONSIDERED**

Substitute Disclosure Statement Form (PTO-1449)

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Jerome M. Eldridge et al.	Examiner:	Tu-Tu Ho
Serial No.:	10/081818	Group Art Unit:	2818
Filed:	February 20, 2002	Docket:	1303.045US1
Title:	ATOMIC LAYER DEPOSITION OF METAL OXIDE AND/OR LOW ASYMMETRICAL TUNNEL BARRIER INTERPLOY INSULATORS		

COMMUNICATION CONCERNING RELATED APPLICATION(S)

Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Applicants would like to bring to the Examiner's attention the following related application(s) in the above-identified patent application:

Serial/Patent No.	Filing Date	Attorney Docket	Title
09/945507	August 30, 2001	1303.014US1	FLASH MEMORY WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS
09/945395	August 30, 2001	1303.019US1	DRAM CELLS WITH REPRESSED FLOATING GATE MEMORY, LOW TUNNEL BARRIER INTERPOLY INSULATORS
09/943134	August 30, 2001	1303.020US1	PROGRAMMABLE ARRAY LOGIC OR MEMORY DEVICES WITH ASYMMETRICAL TUNNEL BARRIERS
09/945498	August 30, 2001	1303.024US1	INTEGRATED CIRCUIT MEMORY DEVICE AND METHOD
09/945512	August 30, 2001	1303.027US1	IN SERVICE PROGRAMMABLE LOGIC ARRAYS WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS
09/945554	August 30, 2001	1303.028US1	SRAM CELLS WITH REPRESSED FLOATING GATE MEMORY, LOW TUNNEL BARRIER INTERPOLY INSULATORS

09/945500	August 30, 2001	1303.029US1	PROGRAMMABLE MEMORY ADDRESS AND DECODE CIRCUITS WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS
10/028001	December 20, 2001	1303.035US1	PROGRAMMABLE ARRAY LOGIC OR MEMORY WITH P-CHANNEL DEVICES AND ASYMMETRICAL TUNNEL BARRIERS
10/177096	June 21, 2002	1303.063US1	GRADED COMPOSITION METAL OXIDE TUNNEL BARRIER INTERPOLY INSULATORS

Respectfully submitted,

JEROME M. ELDRIDGE ET AL.

By Applicants' Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 349-9587

Date 5 Dec '03 By _____
Timothy B. Clise
Reg. No. 40,957

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop RCE, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 5th day of December, 2003.

Name Amy Moriarty Signature _____